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EXAMINER
CHU, CHRIS C

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/757,373	USSERY ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this c mmunication appears on the cover sheet with th c rresp ndence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3 and 5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

In Fig. 3, reference numbers "166" and "156" are not described in the specification.

In Fig. 6c, reference number "220" is not described in the specification.

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "102" has been used to designate both processor and Q-Bus, and reference character "110" has been used to designate both branch control unit and processor task engine. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Specification

4. The disclosure is objected to because of the following informalities:

On page 8, line 24, "processor task engine 110" should be --processor task engine 100--.

On page 14, line 6, "architecture 210" should be -- architecture 220--.

Appropriate correction is required.

Claim Objections

5. Claims 17 and 27 are objected to because of the following informalities:

In claim 17, line 1, "The multi-processor system of claim 1" should be --The processor of claim 1--.

In claim 27, line 1, "The processor of claim 18" should be -- The multi-processor system of claim 18--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 ~ 9, 11, 13, 16 ~ 20, 22, 24, 27, 28, 30, 33 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Ussery et al.

Regarding claim 1, Ussery et al. discloses in Fig. 2, Fig. 5 and column 8, lines 43 ~ 49 a designer configurable processor (200) comprising:

- a. a plurality of designer configurable computational units (218, 220 and 222) operating in parallel;
- b. a memory device (202, 203 and 214) that communicates with the plurality of computational units through a data communication module (206); and
- c. a software development tool (50) that configures the plurality of computational units and a data path though the data communication module.

Regarding claim 2, Ussery et al. discloses in Fig. 5 and column 3, lines 4 ~ 5 the designer configurable processor comprising a Very Long Instruction Word (VLIW) processor task engine.

Regarding claim 3, Ussery et al. discloses in Fig. 5 the data communication module comprising a register routed data communication module.

Regarding claim 4, Ussery et al. discloses in Fig. 5 and column 8, lines 50 ~ 55 the memory device (214) storing at least one of data and instruction code.

Regarding claim 5, Ussery et al. discloses in Fig. 5 and column 8, lines 36 ~ 43 a task queue (208) that communicates with the data communication module, the task queue scheduling tasks for the processor.

Regarding claim 6, Ussery et al. discloses in Fig. 5 the task queue comprising a task queue controller module (212) that communicates with the data communication module and a task queue module that communicates with task queue bus (210).

Regarding claim 7, Ussery et al. discloses in Fig. 5 an instruction memory (214) that communicates with the task queue controller module, the instruction memory storing tasks for the processor.

Regarding claim 8, Ussery et al. discloses in Fig. 2 the software development tool comprising at least one of a compiler (52), an assembler, an instruction set simulator, or a debugging environment.

Regarding claim 9, Ussery et al. discloses in Fig. 2 and column 5, lines 3 ~ 17 the software development tool comprising a graphical interface (62) that visually illustrates the configuration of the processor.

Regarding claim 11, Ussery et al. discloses in Fig. 2 and Fig. 4 the software development tool configuring a data path from the processor to an input/output module.

Regarding claim 13, Ussery et al. discloses in Fig. 2 and Fig. 5 the software development tool configuring a data routing path of at least one of the plurality of computational units.

Regarding claim 16, Ussery et al. discloses in Fig. 2 and Fig. 5 the software development tool configuring an instruction set of at least one of the plurality of computational units.

Regarding claim 17, Ussery et al. discloses in Fig. 2 and Fig. 5 at least one of the plurality of designer configurable computational units (222) comprising a set of input registers and a set of result registers.

Regarding claim 18, Ussery et al. discloses in Fig. 2, Fig. 4 and Fig. 5 a designer configurable multi-processor system comprising:

- a. a plurality of designer configurable processors (152 and 154), each of the plurality of processors comprising a plurality of designer configurable computational units (218, 220 and 222) operating in parallel;
- b. a memory device (202, 203 and 214) that communicates with the plurality of computational units through a data communication module;
- c. an input/output (I/O) module (160) that communicates with at least one of the plurality of processors through an I/O bus; and

d. a software development tool (50) that configures the multi-processor system.

Regarding claim 19, Ussery et al. discloses in Fig. 5 and column 3, lines 4 ~ 5 at least one of the plurality of plurality of processors comprising a Very Long Instruction Word (VLIW) processor.

Regarding claim 20, Ussery et al. discloses in Fig. 4 an instruction memory device (156) that communicates with at least one of the plurality of processors.

Regarding claim 22, Ussery et al. discloses in Fig. 4 the software development tool configuring a data path to the I/O module (160).

Regarding claim 24, Ussery et al. discloses in Fig. 2 and Fig. 5 the software development tool configuring a data routing path of at least one of the plurality of computational units.

Regarding claim 27, Ussery et al. discloses in Fig. 2 and Fig. 5 the software development tool configuring an instruction set of at least one of the plurality of computational units.

Regarding claim 28, Ussery et al. discloses in Fig. 2, Fig. 5 and column 3, lines 4 ~ 5 a method of defining a computational unit for a multi-processor hardware system, the method comprising:

- a. defining an architecture (200) of at least computation unit (218) in a Very Long Instruction Word (VLIW) processor with a software development tool (50); and
- b. generating data from the software development tool that integrates the at least one computation unit into the VLIW processor task engine.

Regarding claim 30, Ussery et al. discloses in Fig. 2 and Fig. 5 defining an internal data routing path of the at least one computation unit with the software development tool.

Regarding claim 33, Ussery et al. discloses in Fig. 2 and Fig. 5 defining an instruction set of the at least one computation unit with the software development tool.

Regarding claim 35, Ussery et al. discloses in Fig. 2 and Fig. 5 the generating data from the software development tool comprising generating scripts for an electronic design automation tool.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ussery et al. in view of Killian et al.

Regarding claim 10, Ussery et al. discloses the claimed invention except for the software development tool generating a synthesizable RTL description of the processor. However, Killian

et al. teaches in column 32, lines 49 ~ 60 a software development tool generating a synthesizable RTL description of a processor. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the synthesizable RTL description as taught by Killian et al. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of obtaining a CPLD implementation (column 32, lines 55 and 56).

Regarding claim 21, Ussery et al. discloses the claimed invention except for the software development tool generating a synthesizable RTL description of at least one of the plurality of processors. However, Killian et al. teaches in column 32, lines 49 ~ 60 a software development tool generating a synthesizable RTL description of at least one of plurality of processors. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the synthesizable RTL description as taught by Killian et al. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of obtaining a CPLD implementation (column 32, lines 55 and 56).

10. Claims 12, 23 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ussery et al. in view of Rupp.

Regarding claim 12, Ussery et al. discloses the claimed invention except for the software development tool configuring a width of the data path from the processor to the input/output module. However, Rupp teaches in column 37, lines 42 ~ 52 a software development tool configuring a width of a data path from a processor to an input/output module. Thus, it would

have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the width of a data path as taught by Rupp. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of defining the memory speed (column 37, lines 46 ~ 48).

Regarding claim 23, Ussery et al. discloses the claimed invention except for the software development tool configures a width of the data path to the I/O module. However, Rupp teaches in column 37, lines 42 ~ 52 a software development tool configuring a width of a data path to an I/O module. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the width of a data path as taught by Rupp. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of defining the memory speed (column 37, lines 46 ~ 48).

Regarding claim 29, Ussery et al. discloses the claimed invention except for defining a data path width of the at least one computation unit with the software development tool. However, Rupp teaches in column 6, lines 4 ~ 13 and column 37, lines 42 ~ 52 defining a data path width of at least one computation unit with a software development tool. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the width of a data path as taught by Rupp. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of defining the memory speed (column 37, lines 46 ~ 48).

11. Claims 14, 25 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ussery et al. in view of Greenbaum et al.

Regarding claims 14 and 25, Ussery et al. discloses the claimed invention except for the software development tool configures an instruction execution speed of at least one of the plurality of computational units. However, Greenbaum et al. teaches in column 3, lines 25 ~ 45 a software development tool configuring an instruction execution speed of at least one of plurality of computational units. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the execution speed as taught by Greenbaum et al. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of providing configurable logic resources into the system (column 3, lines 25 ~ 26).

Regarding claim 32, Ussery et al. discloses the claimed invention except for defining an instruction speed of the at least one computation unit with the software development tool. However, Greenbaum et al. teaches in column 3, lines 25 ~ 45 defining an instruction speed of at least one computation unit with a software development tool. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the execution speed as taught by Greenbaum et al. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of providing configurable logic resources into the system (column 3, lines 25 ~ 26).

12. Claims 15, 26 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ussery et al. in view of Suzuki.

Regarding claims 15 and 26, Ussery et al. discloses the claimed invention except for the software development tool configures an energy required to operate at least one of the plurality of computational units. However, Suzuki teaches in column 4, lines 25 ~ 39 a software development tool configuring an energy required to operate at least one of plurality of computational units. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the energy required as taught by Suzuki. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of executing each of the programs with the computer (column 4, line 25).

Regarding claim 31, Ussery et al. discloses the claimed invention except for defining an energy used to operate the at least one computation unit with the software development tool. However, Suzuki teaches in column 4, lines 25 ~ 39 defining an energy used to operate at least one computation unit with a software development tool. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the energy required as taught by Suzuki. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of executing each of the programs with the computer (column 4, line 25).

13. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ussery et al. in view of Enokido et al.

Regarding claim 12, Ussery et al. discloses the claimed invention except for performing a consistency check to validate the multi-processor hardware system. However, Enokido et al.

teaches in column 2, lines 27 ~ 43 performing a consistency check to validate a multi-processor hardware system. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ussery et al. by using the consistency check as taught by Enokido et al. The ordinary artisan would have been motivated to modify Ussery et al. in the manner described above for at least the purpose of providing an accurate system.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wang discloses a computer system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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c.c.
May 30, 2003